Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL J. LEMMON
and RAJ RAMANUJAN

Appeal No. 1996-1235
Application No. 08/067,262[1]

ON BRIEF

Before STONER, Chief Administrative Patent Judge, and LEE and TORCZON, Administrative Patent Judges.

TORCZON, Administrative Patent Judge.

DECISION ON APPEAL

In this appeal under 35 U.S.C. § 134 from the final rejection of claims 1-59, all of the pending claims, we reverse.

BACKGROUND

Procedural posture of the appeal

Appellants are under an order to show cause (Paper No. 31) why their appeal should not be dismissed for failure to file a timely reply to an order for compliance with 37 CFR § 1.192(c)(1) and (c)(2) (Paper No. 29). Paragraphs (c)(1) and (c)(2) require appellants to identify the real party-in-interest and any related proceedings, respectively. The appeal brief was filed shortly after the effective date of these paragraphs.

[1] Filed 25 May 1993, claiming the benefit of application no. 07/445,994, filed 4 December 1989 (Paper No. 11).

It appears from the record that Compaq Corporation is the real party-in-interest. E.g., Paper No. 32, Resp. to Order, at 2. Rather than delay this appeal over formal requirements, the formal requirements of paragraphs (c)(1) and (c)(2) have been waived in this appeal.[2] Note that waiver of the formal requirements of paragraphs (c)(1) and (c)(2) does not relieve Appellants or their real party-in-interest of any obligation to provide information material to the prosecution of the underlying application, potentially including information about the real party-in-interest and related proceedings. 37 CFR § 1.56; see Refac Int'l, Ltd. v. Lotus Dev. Corp., 81 F.3d 1576, 1581, 38 USPQ2d 1665, 1669 (Fed. Cir. 1996) (Fact that declarants were former employees of assignee was material); In re Berg, 140 F.3d 1428, 1435 nn.7&8, 46 USPQ2d 1226, 1231 nn.7&8 (Fed. Cir. 1998) (Failure to report related proceeding was misleading).

Decision on the merits

The invention is directed to a computer system that transmits portions of a write data block with a preselected number of intervening bus cycles during which a read command is transmitted.

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[2] The Chief Administrative Patent Judge is a member of this panel and is authorized to waive appellate rules. 37 CFR § 1.183; U.S. Patent and Trademark Office, Manual of Patent Examining Procedure § 1002.02(f) (February 2000).

The examiner has rejected (Paper No. 20 (Ex. Ans.) at 3) all pending claims under 35 U.S.C. § 102(e)[3] as anticipated by Gagliardo et al., U.S. Patent No. 5,043,874 (27 Aug. 1991) (filed 3 Feb. 1989) ("Gagliardo").

Appellants have eighteen independent claims. The examiner has rejected all of the independent claims as a single group (Paper No. 20 at 3-4). Appellants state that their claims stand or fall together (Paper 19 (App. Br.) at 3). Appellants only argue the limitations of claim 1 (reproduced in the Appendix), even though the other independent claims have different scopes. In particular, claim 53 (reproduced in the Appendix) is broader than claim 1 with respect to the contested limitation.

DISCUSSION

Claim construction

The starting point for any patentability analysis is the construction of the claim. See Key Pharm. Inc. v. Hercon Labs., 161 F.3d 709, 713, 48 USPQ2d 1911, 1915 (Fed. Cir. 1998) (observing that determining validity first requires claim construction). However, "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy." Vivid Tech., Inc. v. American Sci. & Eng'g., Inc., 200 F.3d 795, 803, 53 USPQ2d 1289, 1294 (Fed. Cir. 1999). Appellants rely on the following limitations in claim 1:

[3] The examiner has withdrawn a second rejection under 35 U.S.C. § 112 of claim 9 (sometimes identified as claim 10) (Paper No. 20 at 2, ¶ 4).

> 1. A method for interleaving a read operation and a write operation on a bus having a bus cycle time in a computer system including the bus and a first device, the method comprising the steps of:
>
> a) operating the first device to transmit a portion of a write data block on the bus during a first period, the first period including at least one bus cycle time;
>
> b) operating the first device to pause for a preselected number of bus cycle times;
>
> c) operating the first device to transmit a read command on the bus during the preselected number of bus cycle times pause; and
>
> d) operating the first device to transmit a further portion of the write data block on the bus during a second period, the second time period including at least one bus cycle time.

During proceedings in the United States Patent and Trademark Office, claims are given their broadest reasonable construction in light of the specification. E.g., In re Sneed, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). The broadest reasonable interpretation of these limitations in claim 1 is that part of a write data block is transmitted, then the write operation is paused for a preselected number of bus cycles during which a read command is transmitted, and then the write operation is completed.

Claim 53 does not have the read-during-write-pause limitation. Instead, claim 53 simply requires that the data block be transmitted in bursts with a preselected number of bus cycles in between.

Anticipation

Anticipation is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of the claimed invention. In re Spada, 911 F.2d 705, 707, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990). Gagliardo does not teach interleaving a read command during a pause in a write operation. The examiner relies on Gagliardo's write-read data operation (20:42-21:18), but in that example, the read operation does not occur until after the write operation is completed. The examiner does not point to a teaching that the read command is transmitted during a pause in the write operation. Gagliardo does teach buffering memory commands while a memory segment is busy (8:12-28), but the examiner has not pointed out a teaching that any of these buffered commands are transmitted or that this transmission would happen within a predetermined number of bus cycles.

Neither the examiner nor Appellants have addressed claim 53 with any specificity. Claim 53 requires that a data block be transmitted for storage in a plurality of bursts with a preselected number of bus cycles between each burst. The examiner has not explained how the portion of Gagliardo that she relies on (20:42-64) teaches the write operation occurring over a plurality of bus cycles with interruptions lasting preselected numbers of bus cycles.

For the foregoing reasons, we find that the examiner has not established anticipation on the record before us.

DECISION

The rejection of all claims on appeal is

REVERSED

BRUCE H. STONER, JR., Chief
Administrative Patent Judge

JAMESON LEE
Administrative Patent Judge

RICHARD TORCZON
Administrative Patent Judge

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cc: Jeffrey A. Pyle
WILLIAMS, MORGAN & AMERSON, P.C.
7676 HILLMONT ST STE 250
HOUSTON TX 77040-6425

APPENDIX

1. A method for interleaving a read operation and a write operation on a bus having a bus cycle time in a computer system including the bus and a first device, the method comprising the steps of:

a) operating the first device to transmit a portion of a write data block on the bus during a first period, the first period including at least one bus cycle time;

b) operating the first device to pause for a preselected number of bus cycle times;

c) operating the first device to transmit a read command on the bus during the preselected number of bus cycle times pause; and

d) operating the first device to transmit a further portion of the write data block on the bus during a second period, the second time period including at least one bus cycle time.

(Paper No. 6 (19 Oct. 1992 Amdt.) at 2 and 3.)

53. A memory module comprising:

(a) a random access memory device having inputs and outputs;

(b) a control logic device having inputs and outputs, the inputs coupled to a bus having a bus cycle time, the outputs being coupled to the random access memory device; [and]

(c) the control logic device providing outputs to the random access memory device causing the random access memory device to store a block of data transmitted on the bus in a plurality of data bursts interspaced by a preselected number of bus cycle times.

(Paper No. 5 (Subst. Spec.) at 53.)